assigning a priority for ownership of the PCI bus to the master based on availability of the data.

2. The method of Claim 1, wherein after the master requests a target, the master is assigned a MEDIUM priority.

3. The method of Claim 1, wherein if the data is not available, then the master is assigned a LOW priority.

4. The method of Claim 1, wherein if the data is available, then the master is assigned a HIGH priority.

5. The method of Claim 1, wherein the target uses delayed transactions to complete a read access.

6. The method of Claim 5, wherein the target integrates a buffer management scheme.

7. The method of Claim 6, wherein the buffer management scheme includes an input/output cache.

8. The method of Claim 1, wherein identifying a target includes sending a request signal from the master to an arbiter.

9. The method of Claim 8, wherein assigning a priority includes sending a modified request signal to the arbiter.

REMARKS

Claims 1-9 are currently pending in this application. Claim 1 has been amended for clarity. In view of the above amendments and following remarks, applicants respectfully submit that the application is in condition for allowance. Applicants therefore, respectfully

request reexamination, reconsideration and allowance of the application.

The Examiner rejected claims 1-9 under 35 U.S.C. 102(e) as being anticipated by Porterfield (U.S. Patent 6,141,715). Applicant respectfully traverses this rejection.

Independent claim 1 recites a method for assigning ownership of a peripheral component interconnect (PCI) bus comprised in part by "determining if data associated with the target is available; and assigning a priority for ownership of the PCI bus to the master based on availability of the data." Applicants respectfully submit that Porterfield does not disclose or suggest the recited element.

Rather, Porterfield discloses a computer system having a PCI-host bridge 16 having a memory arbiter 40 that arbitrates between transaction requests to a memory 18 from a processor 12 via a processor interface 30 and from a PCI bus 20 via a PCI target interface 34. (see FIG. 2). Porterfield further teaches that any arbitration scheme can be used but that "typically a high-priority write transaction request receives priority over a read transaction request which receives priority over a low priority write transaction request. A high-priority write transaction request occurs when the write buffer 39 is full, with all other write transaction requests being low-priority write transaction requests." (Porterfield, col. 4, lines 15-32).

Thus Porterfield discloses an arbitration scheme for controlling transaction requests to a memory and not for gaining control of the PCI bus as recited in the present invention. Further, Porterfield assigns priority in accordance with the availability of write space in a buffer and not as a function of the availability of data from a particular target.

Accordingly, applicants respectfully submit that claim 1 recites a novel and unobvious method over Porterfield and is therefore allowable. Applicants further submit that claims 2-9 that depend

directly or indirectly on claim 1 are allowable as is claim 1 and for additional limitations recited therein.

It is therefore respectfully submitted that pending claims 1-9 are in condition for allowance, and an early notice of allowance is respectfully requested.

Attached hereto is a marked-up version of the changes made to the above-identified application by the current amendment. The attached page is captioned "**Version with markings to show changes made**."

Respectfully submitted,

CHRISTIE, PARKER & HALE, LLP

By _____
Peter A. Nichols
Reg. No. 47,822
626/795-9900

PAN/pan

VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (Amended) A method of assigning ownership of a peripheral component interconnect (PCI) bus, the method including:

identifying a target requested by a master;

determining if data associated with the target is available; and

assigning a priority for ownership of the PCI bus to the master based on availability of the data.

CKS PAS479270.1-*-12/20/02 1:49 PM